NIOS II Web Server Demo

By Terasic Technologies

◈ Introduction

The Altera DE2 Development and Education Board provides an ideal vehicle for learning about digital logic, computer organization, and FPGAs. Featuring an Altera Cyclone II FPGA, the DE2 board offers state-of-the-art technology suitable for university and college laboratory use, a wide range of design projects, as well as sophisticated digital system development.

This application note describes how to build a web server using DE2 board by using a Nios II processor. The following diagram describes the demo setup and connections. The Nios II processor is running LWIP on the MicroC/OS-II RTOS. The web server uses the industry standard sockets interface to TCP/IP. It uses DHCP protocol to requests an valid IP from the Gateway. Users can use a web browser to examine the web page content stored in the Flash memory on the DE2 board.

Please follow the instructions below.
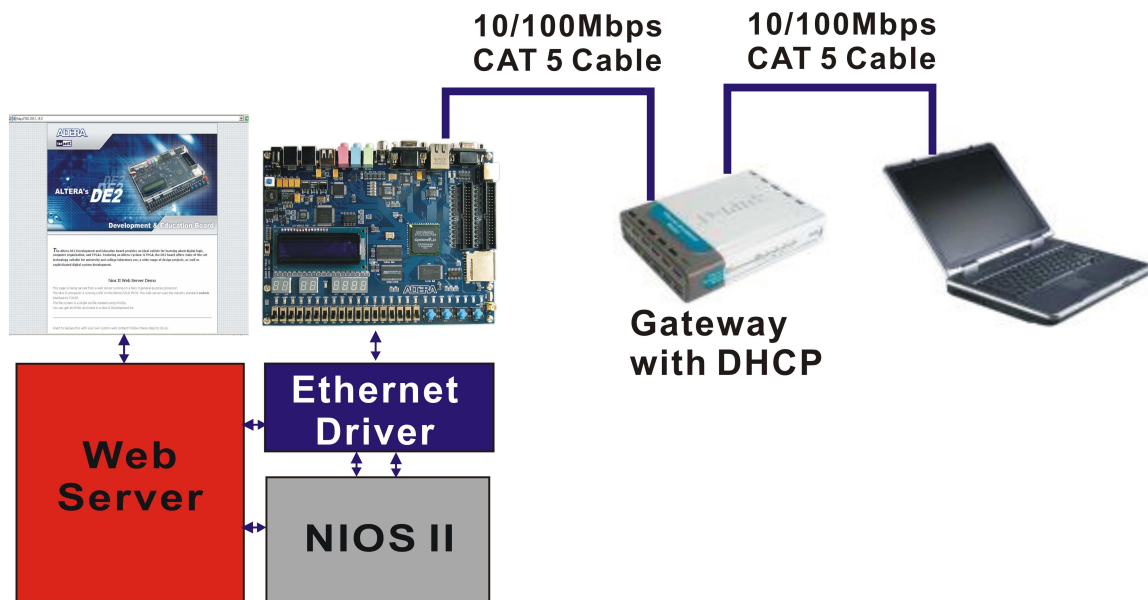
◈ Uncompress the source file and fix the Nios II project path

1. Uncompress the DE2_WEB.rar into a local directory of your choice (use DE2_WEB for this exercise). It is important to ensure that the path to your local directory contains no spaces – otherwise, the Nios II software will not work.

2. Run the DE2_fixpaths.bat batch file. In the dialog box that pops up, select the directory DE2_WEB in your local directory where you uncompressed the files to.
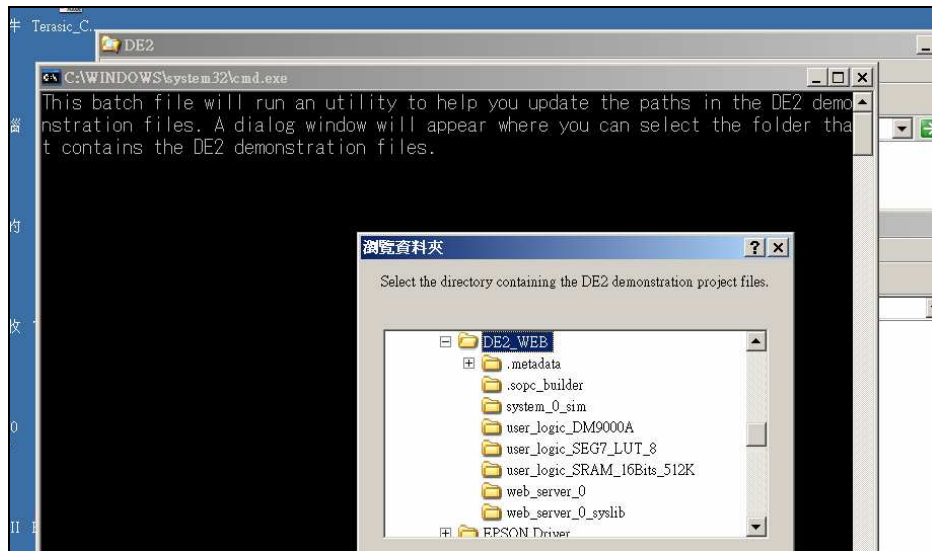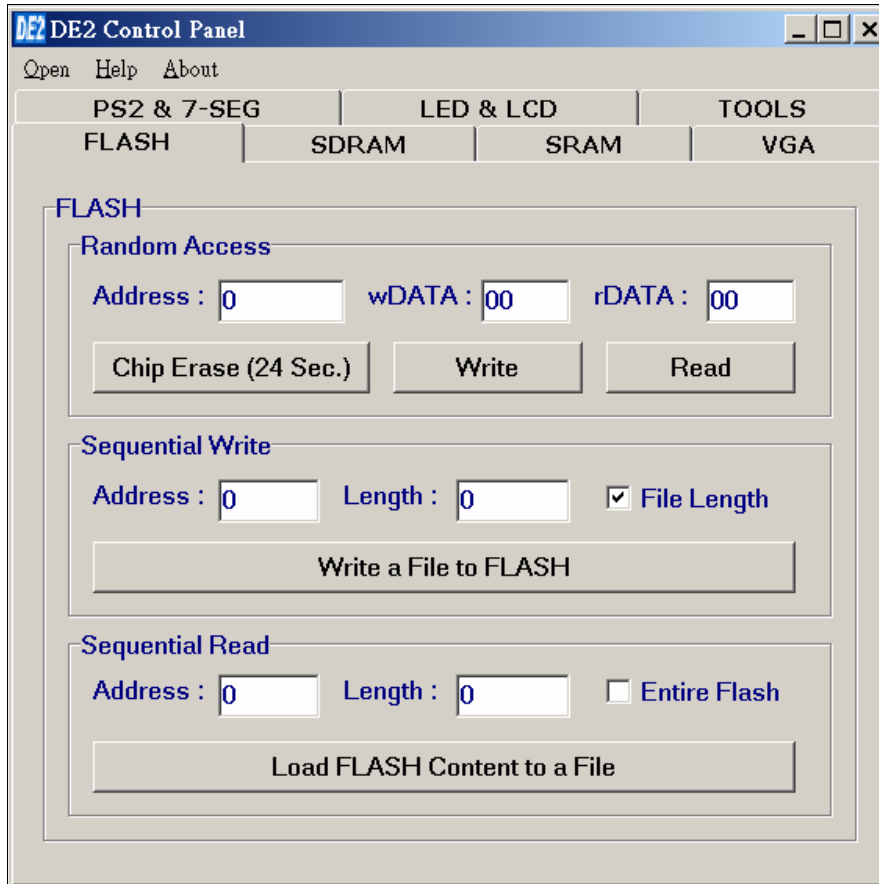
## ◈ Download the web site content into FLASH memory

1. Run the Quartus II and download the DE2 control panel bitstream (USB_API.sof) into FPGA.

2. Execute the DE2_Control_Panel.exe and switch to the FLASH page as shown in the following picture.
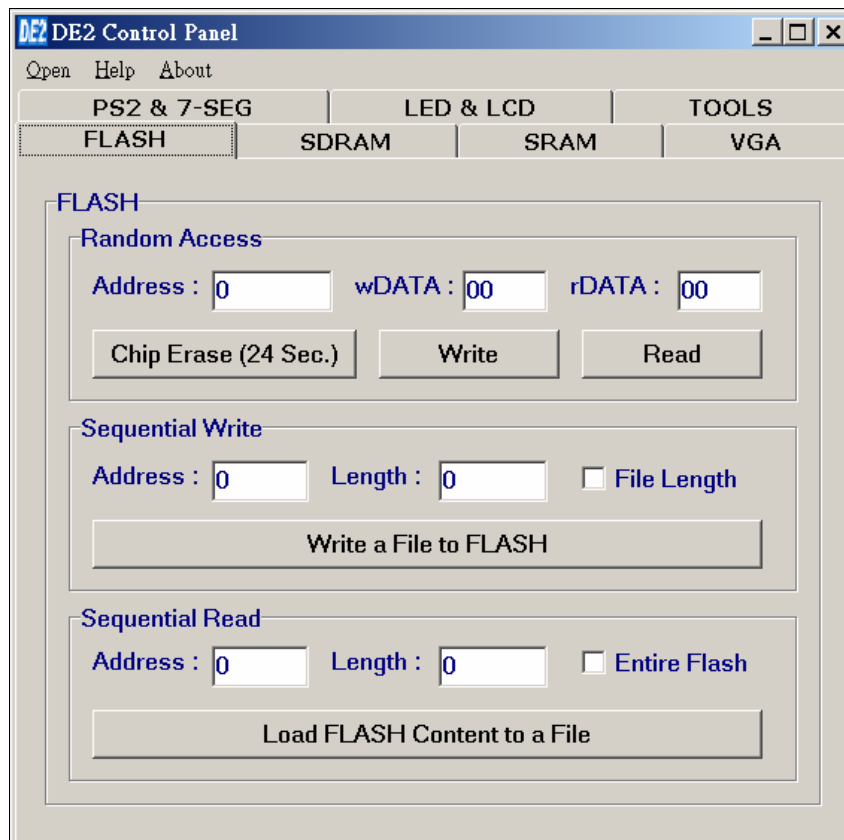
3. Click the "Chip Erase" button to erase the FLASH memory.

4. Select the "File Length" checkbox and confirm the start address is 0.

5. Click the "Write a File to FLASH" button. In the dialog box that pops up, select the ro_zipfs.zip in your local directory (DE2_WEB) where you uncompressed the files to.
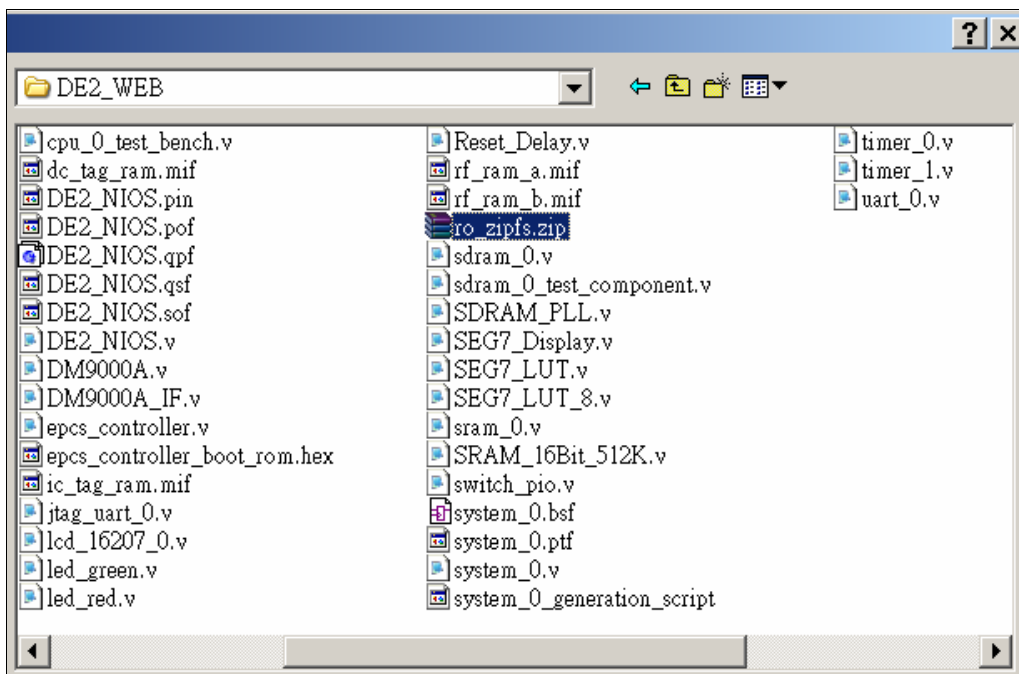

6. Close the DE2 control panel.

◆ Download FPGA bitstream and run the web server

1. Plug a CAT5 cable into the Ethernet port of DE2.

2. Launch Quartus II and download the web server demo bitstream (DE2_NIOS.sof) into FPGA.

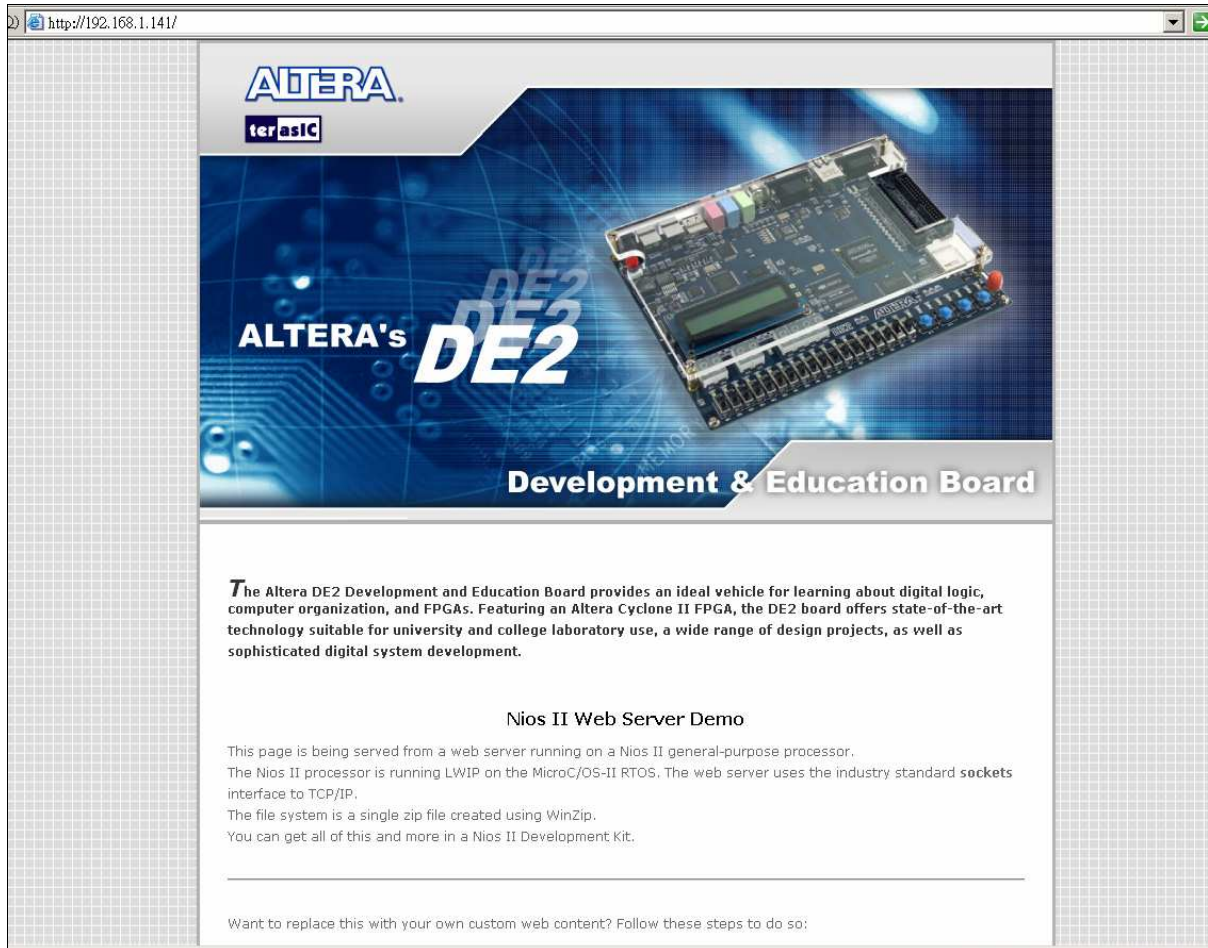3. Launch Nios II IDE and open the DE2_WEB workspace.
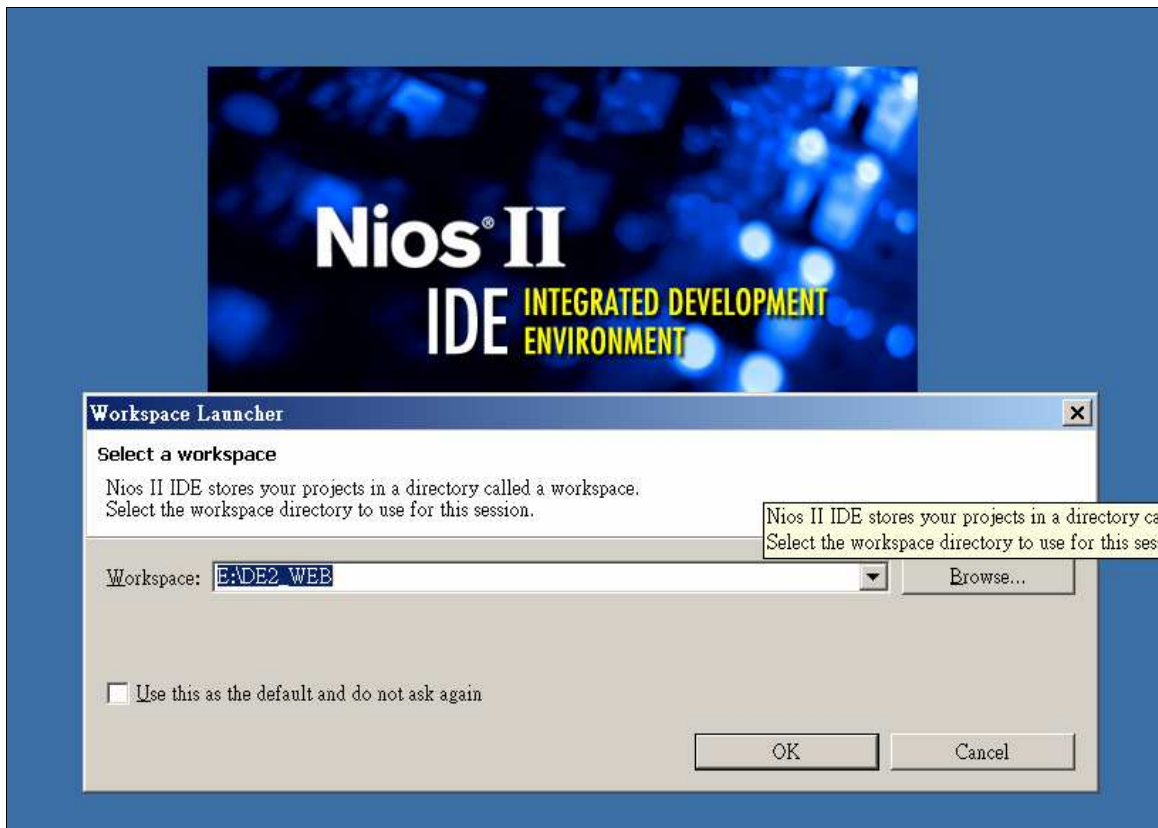
4. Click RUN button to compile this project.

5. When compile is finished, you will see the IP and MAC address show at the LCD display.
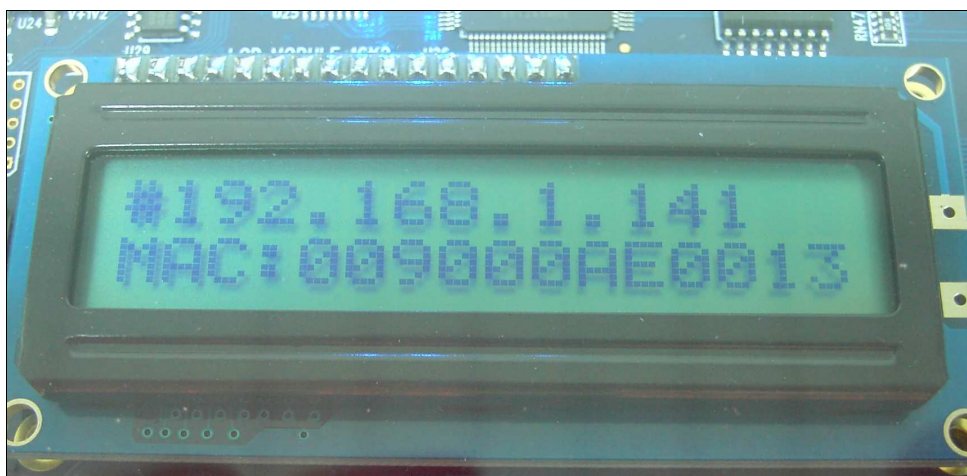
◈ Connect to the DE2 web server

1. Launch your WWW browser.

2. Input the IP into your browser. (IP is shown on the LCD display)

3. Press Enter, you will see the brand new DE2 web page on your computer.

◈ Switch setting

Switch	Function Description
SW[17]	ON, use static IP address. OFF, get IP address from DHCP server.
SW[15:12]	For static IP segment 3.
SW[11:8]	For static IP segment 4.
SW[7:0]	MAC address's lowest byte.

✧ *Static IP address: 192. 168. SW[15:12]. SW[11:8]+128*
✧ *MAC address: 00-90-00-AE-SW[7:0]*